IN THE CLAIMS

Claims 1-26 (canceled).

27. (previously presented) A data processor comprising:

a sequencer which causes a plurality of instructions at a time to be fetched from memory in one fetch cycle, said plurality of instructions using a plurality of arithmetic operation units;

a register for storing data;

the plurality of arithmetic operation units for executing operations based on said plurality of instructions fetched from said memory;

a first plurality of signal lines for sending data stored in said register to said arithmetic operation units;

a second plurality of signal lines for storing data resulting from operation by said arithmetic operation units to said register; and

a bypass circuit for transferring data between different arithmetic operation units when instructions executed by said different arithmetic operation units indicate a same register address.

28. (previously presented) A data processor comprising:

a sequencer which causes a plurality of instructions at a time to be fetched from memory in one fetch cycle, said plurality of instructions using a plurality of arithmetic operation units;

a plurality of registers for storing data;

the plurality of arithmetic operation units for executing operations based on said plurality of instructions fetched from said memory;

a first plurality of signal lines for sending data stored in said registers to said arithmetic operation units;

a second plurality of signal lines for storing data resulting from operation by said arithmetic operation units to said registers; and

a bypass circuit for transferring data between different arithmetic operation units when instructions executed by said different arithmetic operation units indicate a same register address.

29. (previously presented) The data processor according to claim 27, wherein said instructions are consecutive ones to be executed by said different arithmetic operation units.

30. (previously presented) The data processor according to claim 28, wherein said instructions are consecutive ones to be executed by said different arithmetic operation units.

31. (previously presented) A data processor comprising:

a sequencer which causes a plurality of instructions at a time to be fetched from memory in one fetch cycle, said plurality of instructions using a plurality of arithmetic operation units;

a register for storing data;

the plurality of arithmetic operation units for executing operations based on said plurality of instructions fetched from said memory;

a first plurality of signal lines for sending data from said register to an arithmetic operation unit;

a second plurality of signal lines for storing data resulting from operation by an arithmetic operation unit in said register; and

a plurality of switches for connecting said first and second plurality of signal lines to transfer data between different arithmetic operation units when instructions executed by said different arithmetic operation units indicate a same register address.

32. (previously presented) A data processor comprising:

a sequencer which causes a plurality of instructions at a time to be fetched from memory in one fetch cycle, said plurality of instructions using a plurality of arithmetic operation units;

a plurality of registers for storing data;

the plurality of arithmetic operation units for executing operations based on said plurality of instructions fetched from said memory;

a first plurality of signal lines for sending data from a register to an arithmetic operation unit;

a second plurality of signal lines for storing data resulting from operation by an arithmetic operation unit in a register; and

a plurality of switches for connecting said first and second plurality of signal lines to transfer data between different arithmetic operation units when instructions executed by said different arithmetic operation units indicate a same register address.

33. (previously presented) The data processor according to claim 31, wherein said instructions are consecutive ones to be executed by said different arithmetic operation units.

34. (previously presented) The data processor according to claim 32, wherein said instructions are consecutive ones to be executed by said different arithmetic operation units.

35. (previously presented) A data processor comprising:

a sequencer which causes a plurality of instructions at a time to be fetched from memory in one fetch cycle, said plurality of instructions using a plurality of arithmetic operation units;

a register for storing data;

the plurality of arithmetic operation units operable to execute said plurality of instructions fetched from said memory in parallel;

a first group of signal lines for sending data stored in said register to said plurality of arithmetic operation units;

a second group of signal lines for storing data resulting from operation by said arithmetic operation units to said register; and

a bypass circuit for connecting said first group of signal lines and said second group of signal lines,

wherein data resulting from operation by an arithmetic operation unit is not only stored in said register, but also sent to another arithmetic operation unit through said bypass circuit.

Claim 36 (canceled).

37. (previously presented) A data processor comprising:

a sequencer which causes a plurality of instructions at a time to be fetched from memory in one fetch cycle, said plurality of instructions using first and second arithmetic operation units;

a plurality of registers;

the first and second arithmetic operation units for executing operations based on said plurality of instructions fetched from said memory;

first signal lines for transferring data from said registers to said first arithmetic operation unit;

second signal lines for transferring data from said registers to said second arithmetic operation unit;

third signal lines for transferring data from said first arithmetic operation unit to said registers;

fourth signal lines for transferring data from said second arithmetic operation unit to said registers;

a first bypass circuit for transferring data from said third signal lines to said second signal lines; and

a second bypass circuit for transferring data from said fourth signal lines to said first signal lines.

38. (previously presented) The data processor according to claim 35, wherein said bypass circuits comprise switches.

39. (previously presented) The data processor according to claim 36, wherein said bypass circuits comprise switches.

40. (previously presented) The data processor according to claim 37, wherein said bypass circuits comprise switches.